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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,847	09/09/2003	Ai-Sen Liu	24061.142 (TSMC2002-1387)	2138
42717	7590	05/04/2005	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			DUONG, KHANH B	
			ART UNIT	PAPER NUMBER

2822

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

**Office Action Summary**

Application No.

10/657,847

Applicant(s)

LIU ET AL.

Examiner

Khanh B. Duong

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 January 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-74 is/are pending in the application.
- 4a) Of the above claim(s) 30-34 and 61-72 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,3-5,29,60 and 73 is/are allowed.
- 6) ☒ Claim(s) 2,6-10,35-41 and 74 is/are rejected.
- 7) ☒ Claim(s) 11-28 and 42-59 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>1/29/04</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Election/Restrictions***

Applicant's election with traverse of Group II, claims 1-29, 35-60 and 73-74 in the reply filed on January 28, 2005 is acknowledged. The traversal is on the ground(s) that "the embodiments delineated by the examiner are not patentable distinct and therefore constitute a single invention concept". This is not found persuasive because Applicant has not specifically addressed the reason for the restriction requirement as provided by the previous Examiner.

The requirement is still deemed proper and is therefore made FINAL.

Claims 30-34 and 61-72 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim.

### ***Claim Objections***

Claims 56-59 are objected to because of the following informalities: claim 56 depends on claim 57. It should depend on claim 53.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**Claim 74 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Claim 74 recites the limitation "said first dielectric layer" (3 occurrences) in lines 2, 6 and 13. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Ernack et al. (U.S. Patent No. 3,510,369).**

Re claim 2, Ernack et al. ("Ernack") discloses in FIGs. 1-7 a method of making a semiconductor device, comprising: providing a silicon carbide-based barrier 12 layer on a substrate 10; and converting a portion of said silicon carbide-based barrier layer 12 with an oxidation treatment into a layer of silicon oxide 14 [see col. 2, line 11 to col. 3, line 44] .

**Claims 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Loboda et al. (U.S. 5,818,071).**

Re claims 6 and 8, Loboda et al. ("Loboda") discloses in Fig. 1 a method of fabricating a dielectric barrier layer in an integrated circuit structure comprising: providing a low-k interlayer dielectric layer 5 (low-k) on a substrate 1, said dielectric layer 5 having at least one opening exposing an underlying metal layer 3; and forming a first silicon carbide-based barrier layer 8 to conformally cover exposed surfaces of said opening [see col. 3, line 17 to col. 4, line 14].

Loboda further discloses forming a silicon carbide-based barrier layer using a chemical vapor

deposition process or a plasma enhanced chemical vapor deposition process [see col. 2, lines 36-64].

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Loboda in view of Ngo et al. (U.S. 6,723,634).**

Loboda discloses a method of fabricating a dielectric barrier layer in an integrated circuit structure previously as described, which method is repeated herein.

Re claim 7, Loboda fails to disclose the low-k interlayer dielectric layer 5 comprising carbon-doped silicon oxide.

Ngo et al. ("Ngo") suggests materials for low-k interlayer dielectric layer include carbon-doped silicon oxide [see col. 6, lines 30-59].

Since Loboda and Ngo are from the same field of endeavor, the purpose disclosed by Ngo would have been recognized in the pertinent prior art of Loboda.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Loboda as suggested by Ngo, since Ngo states at column 6, lines 30-34 that such material is used to reduce interconnect capacitance.

**Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loboda in view of Li et al. (U.S. 6,790,788).**

Re claims 9 and 10, Loboda fails to disclose said first silicon carbide-based barrier layer is formed to a thickness of from about 200 angstroms to about 400 angstroms, and wherein said first silicon carbide-based barrier layer is formed at a temperature of from about 350°C to about 450°C.

Li et al. ("Li") suggests forming a silicon carbide-based barrier layer to a thickness of from about 100 angstroms to about 500 angstroms [see col. 9, lines 57-61], and wherein said

silicon carbide-based barrier layer is formed at a temperature of from about 0°C to about 500°C.  
[see col. 7, line 11-63].

Since Loboda and Li are from the same field of endeavor, the purpose disclosed by Li would have been recognized in the pertinent prior art of Loboda.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select appropriate temperature range and thickness within the ranges as suggested by Li. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. “Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed ‘critical ranges’ and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation”. *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

**Claims 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ngo et al. (U.S. 6,723,634) in view of Loboda et al. (U.S. 5,818,071).**

Ngo et al. (“Ngo”) discloses in FIGs. 1 and 2 a method of fabricating a dielectric barrier layer in an integrated circuit structure, comprising: providing a first low-k dielectric layer 13 on a substrate 10 having at least one opening 16, said opening 16 having a via hole which exposes an

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underlying metal layer 11 surrounded by said first low-k dielectric layer 13, said first low-k dielectric layer 13 having an etch stop layer 14 (silicon nitride or silicon carbide) formed thereupon, and a trench over said via hole surrounded by a second low-k dielectric layer 15; and forming a first barrier layer 20 (TaN) to conformally cover the exposed surfaces of said opening 16.

Re claims 35-39, Ngo fails to disclose using silicon-carbide based material to form the first barrier layer 20.

Loboda et al. ("Loboda") suggests in Fig. 1 using silicon-carbide based material to form a barrier layer 8 to prevent diffusion of metal from a wiring layer 6 of high conductivity into the surrounding dielectric 5 [see col. 3, line 65 to col. 4, line 1]. Loboda further discloses forming a silicon carbide-based barrier layer using a chemical vapor deposition process or a plasma enhanced chemical vapor deposition process [see col. 2, lines 36-64].

Since Ngo and Loboda are from the same field of endeavor, the purpose disclosed by Loboda would have been recognized in the pertinent prior art of Ngo.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Ngo in the manner as suggested by Loboda because of the desirability to stop diffusion of metal from a wiring layer of high conductivity into the surrounding dielectric.

Re further claim 36, Ngo discloses the etch stop layer 14 includes silicon carbide [see col. 5, lines 45-47].



Re further claims 37 and 38, Ngo discloses the materials for low-k interlayer dielectric layers include carbon-doped silicon oxide [see col. 6, lines 30-59]. Thus, it is understood that the first and second low-k dielectric layers 13 and 15 include carbon-doped silicon oxide.

**Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ngo and Loboda as applied to claims 35-39 above, and further in view of Li et al. (U.S. 6,790,788).**

Re claims 40 and 41, Ngo and Loboda fail to disclose said first silicon carbide-based barrier layer is formed to a thickness of from about 200 angstroms to about 400 angstroms, and wherein said first silicon carbide-based barrier layer is formed at a temperature of from about 350°C to about 450°C.

Li et al. ("Li") suggests forming a silicon carbide-based barrier layer to a thickness of from about 100 angstroms to about 500 angstroms [see col. 9, lines 57-61], and wherein said silicon carbide-based barrier layer is formed at a temperature of from about 0°C to about 500°C. [see col. 7, line 11-63].

Since Ngo, Loboda and Li are from the same field of endeavor, the purpose disclosed by Li would have been recognized in the pertinent prior art of Ngo and Loboda.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select appropriate temperature range and thickness within the ranges as suggested by Li. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an

unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05..

***Allowable Subject Matter***

Claims 11-28 and 42-59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In addition, claims 56-59 would be allowable if rewritten to overcome the objection set forth in this Office action.

Claim 74 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 1, 3-5, 29, 60 and 73 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: none of the prior art of record, taken alone or in combination, fairly shows or suggests all the limitations as claimed.

Re claim 1, none of the prior art of record discloses the following steps in combination with other claimed limitations: *forming a silicon carbide-based barrier layer to cover exposed surfaces of said carbon-doped silicon oxide dielectric layer; converting a portion of said silicon carbide-based barrier layer with an oxidation treatment into a layer of silicon oxide; and using*

*said carbon-doped silicon oxide dielectric layer as a stop layer to remove said layer of silicon oxide.*

Re claim 3, none of the prior art of record discloses the following steps in combination with other claimed limitations: *forming a conformal first barrier layer over exposed surfaces of said opening; converting said first barrier layer above said dielectric layer and over the bottom of said opening into a second barrier layer, said second barrier layer having a removal rate associated with a first etchant that is greater than a removal rate of said first barrier layer associated with said first etchant; and using said first etchant to remove said second barrier layer.*

Re claim 29, none of the prior art of record discloses the following steps in combination with other claimed limitations: *forming a first silicon carbide-based material to conformally cover the exposed surfaces of said opening; converting said first silicon carbide-based barrier layer above said low-k dielectric layer and over the bottom of said opening with an oxidation treatment into a layer of silicon oxide; removing said silicon oxide layer above said low-k dielectric layer and from the bottom of said trench; filling said opening with a conductive layer in electrical contact with said underlying metal layer; removing said conductive layer above said low-k dielectric layer to a predetermined depth below said low-k dielectric layer to define a recess therebelow; forming a second silicon carbide-based barrier layer to cover said recess and above said low-k dielectric layer and said first silicon carbide-based barrier layer so as to encapsulate said conductive layer; converting said second silicon carbide-based barrier layer above said low-k dielectric layer with an oxidation treatment into a layer of silicon oxide; and removing said layer of silicon oxide.*

Re claim 60, none of the prior art of record discloses the following steps in combination with other claimed limitations: *forming a first silicon carbide-based barrier layer to conformally cover the exposed surfaces of said opening; converting said first silicon carbide-based barrier layer above said second low-k dielectric layer, said etch stop layer, and over the bottom of said via hole with an oxidation treatment into a layer of silicon oxide; removing said silicon oxide layer above said second low-k dielectric layer and said etch stop layer, and from the bottom of said via hole; filling said via hole and said trench with a conductive layer in electrical contact with said underlying metal layer; removing said conductive layer above said second low-k dielectric layer to a predetermined depth below said second low-k dielectric layer to define a recess therebelow; forming a second silicon carbide-based barrier layer to cover said recess and above said second low-k dielectric layer and said first silicon carbide-based barrier layer so as to encapsulate said conductive layer; converting said second silicon carbide-based barrier layer above said second low-k dielectric layer with an oxidation treatment into a layer of silicon oxide; and removing said layer of silicon oxide.*

Re claim 73, none of the prior art of record discloses the following steps in combination with other claimed limitations: *forming a first barrier layer to conformally cover the exposed surfaces of said at least one opening; providing an anisotropic treatment to convert said first barrier layer into a second barrier layer on the top surfaces of said at least one opening and over the bottom of said opening, said second barrier layer having a different etching rate from said first barrier layer; removing said second barrier layer; and filling said at least one opening with a conductive material.*

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

You et al. (U.S. 6,577,009) discloses the use of silicon carbide diffusion barrier layer. However, You et al. does not disclose any teaching regarding converting the diffusion barrier layer to a silicon oxide layer.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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